IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15258US06

In the Application of:

Shervin Moloudi et al.

U.S. Serial No.: 09/698,550

Filed: October 27, 2000

For: ADAPTIVE RADIO TRANSCEIVER WITH SUBSAMPLING MIXERS

Examiner: Marceau Milord

Group Art Unit: 2682

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
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Sir:

This paper is an Appeal Brief in support of a Notice of Appeal that was filed on July 11, 2005. A Petition for a One-Month Extension of Time in which to file an Appeal Brief is enclosed, thereby extending the deadline for filing an Appeal Brief to October 11, 2005.

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REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 011595, Frame 0804.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-93 are pending in the present application. Pending claims 1-32, 39-69 and 76-93 stand rejected under 35 U.S.C. § 103(a) and are the subject of this appeal. Pending claims 33-38 and 70-75 are allowed.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide, for example, a mixer that may include, for example, a track and hold circuit and a bandpass circuit. The track and hold circuit may, for example, track and hold a first signal in response to a second signal. The bandpass circuit may be in cooperation with the track and hold circuit a circuit.

Some embodiments according to some aspects of the present invention may provide, for example, a mixer that may include, for example, a track and hold circuit and a bandpass circuit. The track and hold circuit may, for example, track and hold a first signal in response to a second signal. The bandpass circuit may be in cooperation with the track and hold circuit. The track and hold circuit and the bandpass circuit each may

include, for example, a differential circuit. The first and second signals each may be, for example, differential signals. The track and hold circuit may include, for example, a first transistor, a second transistor, a third transistor and a fourth transistor. The first transistor may have, for example, a first input adapted to be coupled to a first one of the first differential signals and a first output to generate a first output signal in response to the first one of the first differential signals. The second transistor may have, for example, a second input adapted to be coupled to the first one of the first differential signals and a second output to generate a second output signal in response to the first one of the first differential signals. The third transistor may have, for example, a third input adapted to be coupled to a second one of the first differential signals and a third output to generate a third output signal in response to the second one of the first differential signals. The fourth transistor may have, for example, a fourth input adapted to be coupled to the second one of the first differential signals and a fourth output to generate a fourth output signal in response to the second one of the first differential signals. The track and the hold circuit may include, for example, a first switch in a path of the first output signal, a second switch in a path of the second output signal, a third switch in a path of the third output signal and a fourth switch in a path of the fourth output signal. The first switch may be controlled, for example, by a first one of the second differential signals. The second switch may be controlled, for example, by a second one of the second differential signals. The third switch may be controlled, for example, by the first one of the second differential signals. The fourth switch may be controlled, for example, by the second one of the second differential signals.

Some embodiments according to some aspects of the present invention may provide, for example, a mixer that may include, for example, a track and hold circuit and a bandpass circuit. The track and hold circuit may have, for example, a signal input, a control input and a mixed signal output. The bandpass circuit may be coupled, for example, to the signal input and the mixed signal output.

Some embodiments according to some aspects of the present invention may provide, for example, a differential mixer that may include, for example, a track and hold circuit and a bandpass circuit. The track and hold circuit may have, for example, a differential signal input, a differential control input and a differential mixed signal output.

The bandpass circuit may be coupled, for example, to the differential signal input and the differential mixed signal output.

Some embodiments according to some aspects of the present invention may provide, for example, a differential mixer that may include, for example, a track and hold circuit and a bandpass circuit. The track and hold circuit may have, for example, a differential signal input, a differential control input and a differential mixed signal output. The bandpass circuit may be coupled, for example, to the differential signal input and the differential mixed signal output. The track and hold circuit may include, for example, a first transistor, a second transistor, a third transistor and a fourth transistor. The first transistor may have, for example, a first input coupled to a first one of the differential signal inputs and a first output. The second transistor may have, for example, a second input coupled to the first one of the differential signal inputs and a second output. The third transistor may have, for example, a third input coupled to a second one of the differential signal inputs, and a fourth transistor having a fourth input coupled to the second one of the differential signal inputs. The track and hold circuit may include, for example, a first switch coupled to the first output, a second switch coupled to the second output, a third switch coupled to the third output and a fourth switch coupled to the fourth output. The first switch may be controlled, for example, by a first one of the differential control inputs. The second switch may be controlled, for example, by a second one of the differential control inputs. The third switch may be controlled, for example, by the first one of the differential control inputs. The fourth switch may be controlled, for example, by the second one of the differential control inputs.

Some embodiments according to some aspects of the present invention may provide, for example, a mixer that may include, for example, track and hold means and limiting means. The track and hold means may, for example, track and hold a first signal in response to a second signal. The limiting means may, for example, limit the response of the track and hold means to a frequency band. The first signal may be, for example, within the frequency band.

ISSUES FOR REVIEW

Whether claims 1-32, 39-69 and 76-93 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,226,509 B1 to Peter John Mole et al. ("Mole") in view of United States Patent No. 6,587,678 B1 to Alyosha C. Molnar et al. ("Molnar").

GROUPING OF CLAIMS

Claims 1-32, 39-69 and 76-93 do not stand or fall together.

Group I. Claims 1-32 and 39-69 stand or fall together.

Group II. Claims 76-93 stand or fall together.

Group III. Claims 33-38 and 70-75 were allowed.

ARGUMENT

I. Group I: Claims 1-32 and 39-69

Claims 1-32 and 39-69 stand rejected under 35 U.S.C. § 103(a) as being obvious over Mole in view of Molnar.

Teaching Each and Every Element

Claim 1 is reproduced below.

> 1. A mixer, comprising:
> a track and hold circuit to track and hold a first signal in response to a second signal; and
> a bandpass circuit in cooperation with the track and hold circuit.

Claim 39 is reproduced below.

> 39. A mixer, comprising:
> a track and hold circuit having a signal input, a control input, and a mixed signal output; and
> a bandpass circuit coupled to the signal input and the mixed signal output.

Claim 61 is reproduced below.

61. A differential mixer, comprising:
a track and hold circuit having a differential signal input, a differential control input, and a differential mixed signal output; and
a bandpass circuit coupled to the differential signal input and the differential mixed signal output.

To maintain an obviousness rejection, each and every element as set forth in independent claims 1, 39 and 61 must be taught or suggested by Mole in view of Molnar. Appellants respectfully submit that each and every element is not taught or suggested by Mole in view of Molnar and that the Board should reverse the rejection.

For example, claims 1, 39 and 61 each recites, in part, a track and hold circuit. In the Office Action of August 9, 2004, the Examiner stated that "[r]egarding claims 1, 5, 23-24, Mole et al discloses a mixer (figs. 3-4), comprising: a track and hold circuit to track and hold a first signal which is the first mixer (46 of fig. 3) which is also the first mixer in response to a second signal (col. 4, lines 1-52; col. 7, lines 12-63)". Office Action of August 9, 2004 at page 2. Similar citations were also made with respect to independent claims 39 and 61. See, e.g., the Office Action Made Final at pages 6 and 9. Thus, the Examiner alleged that mixer 46 of FIG. 3 in Mole was a track and hold circuit.

Appellants in the Response of November 9, 2004 stated that Mole made no specific reference to "tracking" and "holding" or to circuits that track and hold and asked the Examiner to explain specifically where and how Mole taught a track and hold circuit in order to maintain the obviousness rejection.

In the Office Action of May 25, 2005 ("the Office Action Made Final"), the Examiner stated that Appellants' arguments were "not persuasive" and made the rejection final. Despite Appellants' arguments being "not persuasive", the Examiner completely abandoned his allegedly *prima facie* case of obviousness as set forth in the Office Action of August 9, 2004 with respect to Mole and the track and hold circuit. Appellants respectfully draw the attention of the Board to the Office Action Made Final on page 15 in which, for the first time, the Examiner now argued that "Molnar shows a core mixer that comprises switches 62a-62d coupled between input stage 66, and output stage 23. The switches are controlled by the signals. The preprocessor forms the signals a, b, c, d, and d responsive to the phase-split signals A1, B1, A2, and B2 (figs. 10 A-11E; col. 15, lines 1-45)." The Office Action Made Final at page 15.

Accordingly, although Appellants' arguments were deemed "not persuasive", the Examiner completely changed his arguments (1) by abandoning the alleged teachings of Mole with respect to a track and hold circuit; (2) citing for the first time in the Office Action Made Final a new theory of prima facie obviousness based on newly cited figures and text in the specification; and (3) made the rejection final.

Nevertheless, neither Mole nor Molnar, individually or combined, teaches or suggests a track and hold circuit as set forth in claim 1. As the Examiner has admitted in making a new *prima facie* case of obviousness, Mole does not teach or suggest a track and hold circuit. In fact, Mole is silent as to tracking and holding. On the other hand, the Examiner has presented a new *prima facie* case of obviousness based on Molnar and, in particular, FIGS. 10A-11E and col. 15, lines 1-45 of Molnar. However, Molnar does not make up for the teaching deficiencies of Mole. The cited figures according to Molnar relate to an implementation of a mixer. However, the output OUT+, OUT- of the mixer illustrates the fact that the mixer does not track and hold. Appellants respectfully draw the attention of the Board to FIG. 13 of Molnar. The circuit in FIG. 13 of Molnar alternately connects OUT+ with RF+ and RF-. Thus, OUT+ is either allegedly tracking RF+ or RF-. Since it is always allegedly tracking, it is not holding. In addition, the circuit in FIG. 13 of Molnar alternately connects OUT- with RF- and RF+. Thus, OUT- is either allegedly tracking RF- or RF+. Since it is always allegedly tracking, it is not holding. The term "allegedly" emphasizes that Appellants do not necessarily agree with such an interpretation, but merely propose such an allegation for the sake of argument. Thus, the mixer in Molnar does not provide a track and hold circuit.

Since neither Mole nor Molnar, individually or combined, teaches a track and hold circuit, Appellants respectfully request that the Board reverse the rejection of independent claims 1, 39 and 61 and their respective dependent claims (i.e., claims 2-32, 40-60 and 62-69).

Teaching Away

M.P.E.P. § 2145(X)(D)(2) states unequivocally that "[i]t is improper to combine references where the references teach away from their combination". M.P.E.P. §

2145(X)(D)(2) citing, for example, *In re Gurley*, 27 F. 3d 551, 554, 31 U.S.P.Q.2d 1130, 1132 (Fed. Cir. 1994).

According to the Examiner, Molnar teaches "a direct conversion receiver for receiving a first input signal and directly down converting it to baseband frequencies". The Office Action Made Final at page 2. See also, e.g., Molnar title ("Direct Conversion Receiver Employing Subharmonic Frequency Translator Architecture and Related Preprocessor"). Appellants respectfully submit that a direct down conversion is a completely different architecture and process from intermediate frequency (IF) down conversion. Mole directly and specifically teaches away from direct conversion receivers. In fact, the motivation for the Mole invention is to use intermediate frequency (IF) down conversion (as opposed to direct down conversion as taught by Molnar) to avoid many of the disadvantages of direct down conversion such as, for example, the deleterious effects of dc offsets. For example, a significant problem of direct down conversion is that the directly down converted signal band is corrupted by dc offsets (which may be time varying), for example, at the output of a mixer. These dc offsets cannot be filtered out from the desired signal band without removing desired information in the desired signal band. In response to the problem, Mole specifically and directly teaches away from direct down conversion and, instead, adopts an IF down conversion architecture and process.

In the "SUMMARY OF THE PRIOR ART" section, Mole states that there are two "alternative" lines of thought: (1) direct down conversion and (2) IF down conversion. With respect to direct down conversion (i.e., the alternative model used in Molnar, but rejected in Mole), dc offsets "occur at the output of a mixer" and "appear as part of the signal". See Mole at col. 1, lines 63-65. The dc offsets "have the unwanted effect of corrupting data integrity". See Mole at col. 1, lines 65-66. Furthermore, "[u]nfortunately, these dc offsets cannot be filtered out without removing wanted information in the RF signal. Consequently, the sensitivity of a receiver is limited by the level of the dc offsets." See Mole at col. 1, line 67 and col. 2, lines 1-3. To overcome the problem of dc offsets, Mole rejects direct down conversion and, instead, adopts IF down conversion. With respect to IF down conversion (i.e., the alternative model used in Mole), Mole states that IF down conversion is an "alternative line of thought with respect

to information recovery from a modulated carrier". See Mole at col. 2, lines 8-9. Mole further explains that "the IF signal, whilst being at reduced frequency relative to the carrier, still has a relatively large frequency displacement with respect to baseband (dc)". See Mole at col. 2, lines 11-13. Thus, the dc offsets can be filtered from the desired signal band.

In addition, Molnar directly and specifically teaches away from IF down conversion as taught by Mole. In the BACKGROUND section, Molnar describes the advantages of down conversion receivers over IF down conversion receivers as well as the disadvantages of IF down conversion receivers. Molnar states that direct conversion receivers eliminate extra components of IF down conversion receivers such as IF filters, additional mixers and additional local oscillators. See, e.g., Molnar at col. 2, lines 1-3. Furthermore, Molnar disparages IF technology as "bulky, expensive, and not implementable on-chip". See Molnar at col. 2, lines 4-6. These are but a few of the reasons why Molnar rejects IF down conversion architectures and processes (which are espoused by Mole) and, ultimately, adopts direct down conversion architectures and processes.

Since Molnar specifically and directly teaches away from Mole and since Mole specifically and directly teaches away from Molnar, Mole cannot be properly combined with Molnar. It is therefore respectfully submitted that an obviousness rejection based on the combination of Mole and Molnar cannot be maintained.

For at least the above, it is respectfully requested that the Board reverse the rejection of independent claims 1, 39 and 61 and their respective dependent claims (i.e., claims 2-32, 40-60 and 62-69).

<u>Examiner's Rebuttal to Teaching Away Arguments in the Office Action Made Final</u>

In the Advisory Action, the Examiner failed to address each and every issue raised by Appellants' Response of May 25, 2005 to the Office Action Made Final and instead relied on inapplicable case law. In the Office Action Made Final, the Examiner stated:

> In response to applicant's argument that 'Molnar directly and specifically teaches away from IF down conversion as taught by Mole', it is noted that the features upon which applicant relies (direct down

> conversion and IF conversion) are not recited in the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)."

The Office Action Made Final at page 15.

Appellants note that the following with respect to the Examiner's response: (1) Determining whether two references teach away from each other can be independent of the recited claim elements. (2) *In re Van Geuns* relates to claim interpretation and not to whether two references teach away from each other. Thus, both reasons set forth by the Examiner for refusing to even consider the direct and specific teachings of Molnar and Mole that directly and specifically teach away from each other were incorrect and unresponsive.

Appellants respectfully submit that the Examiner confused two different concepts in patent practice and procedure, namely, claim interpretation and the prohibition against combining references that teach away. The two are separate considerations.

For example, the motivation alleged by the Examiner for combining Mole and Molnar is "to improve noise performance and achieve a higher conversion gain".

Applying the Examiner's own logic and argument, the Examiner would be hard pressed to find such elements as "to improve noise performance and achieve a higher conversion gain" among the recited elements of the claims. Such elements are not recited in any of the claims.

Of course, the Examiner is entitled to provide evidence in Mole and Molnar that is not recited in the claims as a justification or motivation for <u>combining</u> Mole and Molnar.

Similarly, Appellants are entitled to provide evidence in Mole and Molnar that is not recited in the claims as a justification or motivation for <u>not</u> <u>combining</u> Mole and Molnar.

In other words, Appellants are entitled to provide evidence in Mole and Molnar that Mole and Molnar, for example, teach away from each other. In the Advisory Action, the Examiner evidently found such an argument unpersuasive since, in maintaining the rejection, the Examiner merely alleged that all the recited claim elements were in Mole and Molnar. Such a basis for maintaining the obviousness rejection, ignores Appellants

teaching away arguments and ignores M.P.E.P. § 2145(X)(D)(2). The Examiner also chose to ignore Appellants' citation to, for example, *In re Wesslau*, 353 F.2d 238, 241 (C.C.P.A. 1965) which warned examiners that "[i]t is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art."

For at least the above reasons, the Examiner should have fully considered all of the rebuttal evidence and argument made by Appellants.

For at least the above, it is respectfully requested that the Board reverse the rejection of independent claims 1, 39 and 61 and their respective dependent claims (i.e., claims 2-32, 40-60 and 62-69).

The Examiner's citation to *In re Van Geuns* in the Office Action Made Final was an unresponsive and improper response to Appellants' rebuttal evidence and arguments that Mole and Molnar directly and specifically teaches away from each other. Appellants had strongly urged the Examiner to re-read the case.

Appellants respectfully submit that a fair reading of *In re Van Geuns* is that the cited text from *In re Van Geuns* relates to claim interpretation and not to the improper combination of two references in view of direct and specific rebuttal evidence and arguments supporting the fact that the two references teach away from each other.

Appellants have reproduced the relevant text from *In re Van Geuns* that provides the proper context of the quote applied by the Examiner.

> Van Geun's claim 42 recites a magnet assembly with a "uniform magnetic field." The board found that the Japanese reference disclosed a magnet assembly with a substantially uniform magnetic field, varying no more than 10 percent. Van Geuns does not disagree with this finding. Instead, Van Geuns argues that the uniform magnetic field limitation of claim 42 must be interpreted in light of the specification and the understanding of persons skilled in the NMR art and MRI art. Van Geuns then contends that the Japanese reference does not make the invention of claim 42 obvious because it does not teach the level of magnetic field uniformity required for NMR imaging. The short answer is that claim 42 is not expressly limited to NMR or MRI apparatus. In the patentability context, claims are to be given their broadest reasonable interpretations.... Moreover, limitations are not to be read into the claims from the specification.... Thus, Van Geuns cannot read an NMR limitation into

> claim 42 to justify his argument as to the meaning of the "uniform magnetic field."

In re Van Geuns, 988 F.2d at 1184-1185.

As Appellants have pointed out, in relevant part, the cited text in *In re Van Geuns* does not relate to a determination as to whether two references that teach away from each other can be combined, but instead relates to claim interpretation and, in particular, an inventor's attempt to narrow the meaning of the phrase "uniform magnetic field" recited in claim 42 in view of the NMR and MRI arts as described in the specification.

Thus, the cited text in *In re Van Geuns* was an unresponsive and improper response to Appellants' rebuttal evidence and arguments that Mole and Molnar directly and specifically teach away from each other and, thus, were improperly combined.

For at least the above, it is respectfully requested that the Board reverse the rejection of independent claims 1, 39 and 61 and their respective dependent claims (i.e., claims 2-32, 40-60 and 62-69).

<u>Prohibition Against Changing Principle of Operation of Prior Art Invention</u>

M.P.E.P. § 2143.02 states that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." M.P.E.P. § 2143.02 citing, for example, *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959).

Appellants respectfully submit that direct down conversion principles and IF down conversion principles are mutually exclusive principles. Mole refers to the two principles as alternative lines of thought. See, e.g., Mole at col. 1, lines 59-61. Mole emphasizes IF down conversion principles and rejects direct down conversion principles. Molnar emphasizes direct down conversion principles and rejects IF down conversion principles. To modify one in view of the other would inevitably change the principle of operation of the prior art invention being modified. As the prohibition of M.P.E.P. § 2143.02 makes clear, such a modification is not allowed and the teachings of Mole and Molnar are insufficient to render the claims *prima facie* obvious. It is therefore

respectfully submitted that an obviousness rejection based on the combination of Mole and Molnar cannot be maintained.

The Examiner also states that the alleged motivation for combining the direct down conversion arrangement of Molnar with the IF down conversion arrangement of Mole was "to improve noise performance and achieve a higher conversion gain". As is clearly described in Mole, Mole adopts an IF down conversion arrangement to avoid the corruption of data integrity which occurs in the direct down conversion arrangement. See, e.g., Mole at col. 1, lines 59-67 and col. 2, lines 1-3. Thus, combining the direct down conversion arrangement of Molnar with the IF down conversion arrangement of Mole would, in fact, degrade noise performance which is in direct contradistinction with the Examiner's motivation for combining Molnar and Mole.

For at least the above, it is respectfully requested that the Board reverse the rejection of independent claims 1, 39 and 61 and their respective dependent claims (i.e., claims 2-32, 40-60 and 62-69).

Examiner's Rebuttal To Prohibition Against Changing Principle of Operation

In response to Appellants' citation to M.P.E.P. § 2143.02 and the prohibition against changing the principle of operation of Mole, the Examiner in the Office Action Made Final incorrectly addressed the issues raised. In the Office Action Made Final, the Examiner stated that

> [i]n response to applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art could be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975).

The Office Action Made Final at page 15.

Appellants did not argue "that there is no suggestion to combine the references". In fact, Appellants did not argue that "[i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification" as set forth in M.P.E.P. § 2143.01.

Instead, Appellants argued that "[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." Response of May 25, 2005 to the Office Action Made Final at page 18. This argument is completely different and separate from the prohibition against modifying a reference such that it becomes unsatisfactory for its intended purpose.

Thus, the Examiner did not respond to or otherwise appreciate the totality of Appellants' rebuttal evidence and arguments as set forth in the Response to the Office Action Made Final at pages 18-19. In addition to this error, the Examiner in the Advisory Action chose to ignore the prohibition under M.P.E.P. § 2143.01 and merely alleged that all the recited elements were in Mole and Molnar, which is neither dispositive nor responsive.

For at least the above, it is respectfully requested that the Board reverse the rejection of independent claims 1, 39 and 61 and their respective dependent claims (i.e., claims 2-32, 40-60 and 62-69).

II. Group II: Claims 76-93

Claims 76-93 stand rejected under 35 U.S.C. § 103(a) as being obvious over Mole in view of Molnar.

Claim 76 is reproduced below.

> 76. A mixer, comprising:
>
> track and hold means for tracking and holding a first signal in response to a second signal; and
>
> limiting means for limiting the response of the track and hold means to a frequency band, the first signal being within the frequency band.

To maintain an obviousness rejection, each and every element as set forth in independent claim 76 must be taught or suggested by Mole in view of Molnar. Appellants respectfully submit that each and every element is not taught or suggested by Mole in view of Molnar.

For example, claim 76 recites, in part, track and hold means for tracking and holding. Appellants respectfully submit that, since neither Mole nor Molnar, individually

or combined, teaches or suggests a track and hold circuit as set forth in claims 1, 39 and 61, neither Mole nor Molnar, individually or combined, teaches or suggests track and hold means for tracking and holding as set forth in claim 76.

Appellants respectfully submit that the same or similar arguments made with respect to claims 1, 39 and 61 are hereby made with respect to claim 76.

For at least the above, it is respectfully requested that the Board reverse the rejection of independent claim 76 and its dependent claims (i.e., claims 77-93).

III. Group III: Claims 33-38 and 70-75

Claims 33-38 and 70-75 are pending and were allowed.

IV. Conclusion

For the foregoing reasons, claims 1-32, 39-69 and 76-93 are patentable over the prior art of record. Claims 33-38 and 70-75 were previously allowed by the Examiner. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 11, 2005

Respectfully submitted,

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APPENDIX

The following claims are pending in the present application. Claims 33-38 and 70-75 were previously allowed by the Examiner. The rejection of claims 1-32, 39-69 and 76-93 is being appealed.

1. A mixer, comprising:

a track and hold circuit to track and hold a first signal in response to a second signal; and

a bandpass circuit in cooperation with the track and hold circuit.

2. The mixer of claim 1 further comprising an input circuit to buffer the first signal before being applied to the track and hold circuit.

3. The mixer of claim 1 wherein the track and hold circuit comprises first and second output signals, the mixer further comprising a buffer to combine the first and second output signals.

4. The mixer of claim 1 wherein the bandpass circuit comprises an inductor and capacitor each being coupled to the track and hold circuit, the inductor and capacitor cooperating to provide a time constant related to a frequency of the first signal.

5. The mixer of claim 1 wherein the track and hold circuit comprises a switch in a path of the first signal, the switch being controlled by the second signal.

6. The mixer of claim 5 wherein the switch comprises a transistor having a gate coupled to the second signal.

7. The mixer of claim 6 wherein the transistor further comprises a source coupled to the first signal.

8. The mixer of claim 7 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

9. The mixer of claim 8 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

10. The mixer of claim 9 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

11. The mixer of claim 7 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

12. The mixer of claim 11 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

13. The mixer of claim 12 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

14. The mixer of claim 1 wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals.

15. The mixer of claim 14 wherein the track and hold circuit further comprises a first switch in a first path of a first one of the first differential signals and a second switch in a second path of the first one of the first differential signals, the first switch being controlled by a first one of the second differential signals and the second switch being controlled by a second one of the second differential signals.

16. The mixer of claim 15 wherein the track and hold circuit further comprises a third switch in a first path of a second one of the first differential signals and a fourth switch in a fourth path of the second one of the first differential signals, the third switch

being controlled by the first one of the second differential signals and the fourth switch being controlled by a second one of the second differential signals.

17. The mixer of claim 16 wherein the first switch comprises a transistor having a gate coupled to the first one of the second differential signals, the second switch comprises a second transistor having a gate coupled to the second one of the second differential signals, the third switch comprises a third transistor having a gate coupled to the first one of the second differential signals, and the fourth switch comprises a fourth transistor having a gate coupled to the second one of the second differential signals.

18. The mixer of claim 17 wherein the transistors each further comprises a source, the sources of the first and second transistors each being coupled to the first one of the first differential signals and the sources of the third and fourth transistors each being coupled to the second one of the first differential signals.

19. The mixer of claim 18 wherein the bandpass circuit comprises first, second, third and fourth capacitors, wherein the transistors each further comprises a drain, the drain of the first transistor being coupled to the first capacitor, the drain of the second transistor being coupled to the second capacitor, the drain of the third transistor being coupled to the third capacitor, and the drain of the fourth transistor being coupled to the fourth capacitor.

20. The mixer of claim 19 wherein the bandpass circuit further comprises first and second inductors, the first inductor being coupled to the sources of the first and second transistors and the second inductor being coupled to the sources of the third and fourth transistors.

21. The mixer of claim 20 further comprising an input circuit including fifth and sixth transistors each having a drain, the drain of the fifth transistor being coupled to the sources of the first and second transistors and the drain of the sixth transistor being coupled to the sources of the third and fourth transistors.

22. The mixer of claim 18 wherein the first, second, third and fourth transistors each further comprises a drain, the mixer further comprising a buffer to convert voltages at the drains of the first and fourth transistors to a first current and voltages at the drains of the second and third transistors to a second current.

23. The mixer of claim 1 wherein the track and hold circuit comprises a transistor having an input adapted to be coupled to the first signal and an output to generate an output signal in response to the first signal, and a switch in a path of the output signal, the switch being controlled by the second signal.

24. The mixer of claim 23 wherein the switch comprises a second transistor having a gate coupled to the second signal.

25. The mixer of claim 24 wherein the second transistor further comprises a drain coupled to the output of the transistor.

26. The mixer of claim 25 wherein the bandpass circuit comprises a capacitor coupled to the output of the transistor.

27. The mixer of claim 26 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

28. The mixer of claim 27 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

29. The mixer of claim 25 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

30. The mixer of claim 29 wherein the bandpass circuit comprises a capacitor coupled to the output of the transistor.

31. The mixer of claim 30 wherein the capacitor and inductor cooperate to provide a time constant related to a frequency of the first signal.

32. The mixer of claim 1 wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals.

33. A mixer, comprising:

a track and hold circuit to track and hold a first signal in response to a second signal; and

a bandpass circuit in cooperation with the track and hold circuit,

wherein the track and hold circuit and the bandpass circuit each comprises a differential circuit, the first and second signals each being differential signals,

wherein the track and hold circuit comprises a first transistor having a first input adapted to be coupled to a first one of the first differential signals and a first output to generate a first output signal in response to the first one of the first differential signals, a second transistor having a second input adapted to be coupled to the first one of the first differential signals and a second output to generate a second output signal in response to the first one of the first differential signals, a third transistor having a third input adapted to be coupled to a second one of the first differential signals and a third output to generate a third output signal in response to the second one of the first differential signals, and a fourth transistor having a fourth input adapted to be coupled to the second one of the first differential signals and a fourth output to generate a fourth output signal in response to the second one of the first differential signals, wherein the track and the hold circuit further comprises a first switch in a path of the first output signal, a second switch in a path of the second output signal, a third switch in a path of the third output signal, and a fourth switch in a path of the fourth output signal, the first switch being controlled by a first one of the second differential signals, the second switch being controlled by a second

one of the second differential signals, the third switch being controlled by the first one of the second differential signals, and the fourth switch being controlled by the second one of the second differential signals.

34. The mixer of claim 33 wherein the first switch comprises a fifth transistor having a gate coupled to the first one of the second differential signals, the second switch comprises a sixth transistor having a gate coupled to the second one of the second differential signals, the third switch comprises a seventh transistor having a gate coupled to the first one of the second differential signals, and the fourth switch comprises an eighth transistor having a gate coupled to the second one of the second differential signals.

35. The mixer of claim 34 wherein the bandpass circuit further comprises a first capacitor coupled to the first output of the first transistor, a second capacitor coupled to the second output of the second transistor, a third capacitor coupled to the third output of the third transistor, and a fourth capacitor coupled to the fourth output of the fourth transistor.

36. The mixer of claim 35 wherein the fifth, sixth, seventh and eighth transistors each comprises a drain and source, the drain of the fifth transistor being coupled to the first capacitor, the drain of the sixth capacitor being coupled to the second capacitor, the drain of the seventh transistor being coupled to the third capacitor, and the drain of the eighth transistor being coupled to the fourth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, a second inductor coupled to the drain of the sixth transistor, a third inductor coupled to the drain of the seventh transistor, and a fourth inductor coupled to the drain of the eighth transistor.

37. The mixer of claim 36 wherein each of the first, second, third and fourth transistors comprises a source, the source of the first and third transistors being coupled

together and the sources of the second and fourth transistors being coupled together, the mixer further comprising a fifth switch coupled to the common sources of the first and third transistors, and a sixth switch coupled to the common sources of the second and fourth transistors, the fifth switch being controlled by the first one of the second differential signals and the sixth switch being controlled by the second one of the second differential signals.

38. The mixer of claim 37 further comprising a buffer to convert voltages at the first and fourth outputs to a first current and voltages at the second and third outputs to a second current.

39. A mixer, comprising:

a track and hold circuit having a signal input, a control input, and a mixed signal output; and

a bandpass circuit coupled to the signal input and the mixed signal output.

40. The mixer of claim 39 further comprising an input circuit coupled to the signal input.

41. The mixer of claim 39 wherein the mixed signal output comprises first and second output signals, the mixer further comprising a buffer to combine the first and second output signals.

42. The mixer of claim 39 wherein the bandpass circuit comprises an inductor coupled to the signal input and a capacitor coupled to the mixed signal output.

43. The mixer of claim 39 wherein the track and hold circuit comprises a switch between the signal input and the mixed signal output, the switch being controlled by the control input.

44. The mixer of claim 43 wherein the switch comprises a transistor having a gate coupled to the control input.

45. The mixer of claim 44 wherein the transistor further comprises a source coupled to the signal input.

46. The mixer of claim 45 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

47. The mixer of claim 46 wherein the bandpass circuit further comprises an inductor coupled to the signal input.

48. The mixer of claim 47 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

49. The mixer of claim 45 wherein the bandpass circuit further comprises an inductor coupled to the signal input.

50. The mixer of claim 49 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

51. The mixer of claim 50 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

52. The mixer of claim 39 wherein the track and hold circuit comprises a transistor having an input coupled to the signal input and an output coupled to the mixed signal output, and a current source coupled to the mixed signal output, the current source being controlled by the control input.

53. The mixer of claim 52 wherein the current source comprises a second transistor having a gate coupled to the control input.

54. The mixer of claim 53 wherein the second transistor further comprises a drain coupled to the mixed signal output.

55. The mixer of claim 54 wherein the bandpass circuit comprises a capacitor coupled to the mixed signal output.

56. The mixer of claim 55 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the drain of the second transistor.

57. The mixer of claim 56 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

58. The mixer of claim 55 wherein the second transistor further comprises a source, and the bandpass circuit further comprises an inductor coupled to the source of the second transistor.

59. The mixer of claim 58 wherein the bandpass circuit comprises a capacitor coupled to the mixed signal output.

60. The mixer of claim 59 wherein the capacitor and inductor cooperate to provide a time constant related to a signal frequency applied to the signal input.

61. A differential mixer, comprising:

a track and hold circuit having a differential signal input, a differential control input, and a differential mixed signal output; and

a bandpass circuit coupled to the differential signal input and the differential mixed signal output.

62. The mixer of claim 61 wherein the track and hold circuit further comprises a first switch between a first one of the differential inputs and a first one of the differential mixed signal outputs, and a second switch between the first one of the differential inputs and the first one of the differential mixed signal outputs, the first switch being controlled by a first one of the differential control inputs and the second switch being controlled by a second one of the differential control inputs.

63. The mixer of claim 62 wherein the track and hold circuit further comprises a third switch between a second one of the differential inputs and a second one of the differential mixed signal outputs, and a fourth switch between the second one of the differential inputs and the second one of the differential mixed signal outputs, the third switch being controlled by a first one of the differential control inputs and the fourth switch being controlled by a second one of the differential control inputs.

64. The mixer of claim 63 wherein the first switch comprises a transistor having a gate coupled to the first one of the differential control inputs, the second switch comprises a second transistor having a gate coupled to the second one of the differential control inputs, the third switch comprises a third transistor having a gate coupled to the first one of the differential control inputs, and the fourth switch comprises a fourth transistor having a gate coupled to the second one of the differential control inputs.

65. The mixer of claim 64 wherein the transistors each further comprises a source, the sources of the first and second transistors each being coupled to the first one of the differential signal inputs and the sources of the third and fourth transistors each being coupled to the second one of the differential signal inputs.

66. The mixer of claim 65 wherein the bandpass circuit comprises first, second, third and fourth capacitors, wherein the transistors each further comprises a drain, the drain of the first transistor being coupled to the first capacitor, the drain of the second transistor being coupled to the second capacitor, the drain of the third transistor

being coupled to the third capacitor, and the drain of the fourth transistor being coupled to the fourth capacitor.

67. The mixer of claim 66 wherein the bandpass circuit further comprises first and second inductors, the first inductor being coupled to the sources of the first and second transistors and the second inductor being coupled to the sources of the third and fourth transistors.

68. The mixer of claim 67 further comprising an input circuit including fifth and sixth transistors each having a drain, the drain of the fifth transistor being coupled to the sources of the first and second transistors and the drain of the sixth transistor being coupled to the sources of the third and fourth transistors.

69. The mixer of claim 68 wherein the first, second, third and fourth transistors each further comprises a drain, the mixer further comprising a buffer to convert voltages at the drains of the first and fourth transistors to a first current and voltages at the drains of the second and third transistors to a second current.

70. A differential mixer, comprising:

a track and hold circuit having a differential signal input, a differential control input, and a differential mixed signal output; and

a bandpass circuit coupled to the differential signal input and the differential mixed signal output,

wherein the track and hold circuit comprises a first transistor having a first input coupled to a first one of the differential signal inputs and a first output, a second transistor having a second input coupled to the first one of the differential signal inputs and a second output, a third transistor having a third input coupled to a second one of the differential signal inputs, and a fourth transistor having a fourth input coupled to the second one of the differential signal inputs, wherein the track and hold circuit further comprises a first switch coupled to the first output, a second switch coupled to the second output, a third switch coupled to the third output, and a fourth switch coupled to the

fourth output the first switch being controlled by a first one of the differential control inputs, the second switch being controlled by a second one of the differential control inputs, the third switch being controlled by the first one of the differential control inputs, and the fourth switch being controlled by the second one of the differential control inputs.

71. The mixer of claim 70 wherein the first switch comprises a fifth transistor having a gate coupled to the first one of the differential control inputs, the second switch comprises a sixth transistor having a gate coupled to the second one of the differential control inputs, the third switch comprises a seventh transistor having a gate coupled to the first one of the differential control inputs, and the fourth switch comprises an eighth transistor having a gate coupled to the second one of the differential control inputs.

72. The mixer of claim 71 wherein the bandpass circuit further comprising a first capacitor coupled to the first output of the first transistor, a second capacitor coupled to the second output of the second transistor, a third capacitor coupled to the third output of the third transistor, and a fourth capacitor coupled to the fourth output of the fourth transistor.

73. The mixer of claim 72 wherein the firth, sixth, seventh, and eighth transistors each comprises a drain and source, the drain of the firth transistor being coupled to the first capacitor, the drain of the sixth capacitor being coupled to the second capacitor, the drain of the seventh transistor being coupled to the third capacitor, and the drain of the eighth transistor being coupled to the fourth transistor, the bandpass circuit further comprising a first inductor coupled to the drain of the fifth transistor, a second inductor coupled to the drain of the sixth transistor, a third inductor coupled to the drain of the seventh transistor, and a fourth inductor coupled to the drain of the eighth transistor.

74. The mixer of claim 73 wherein each of the first, second, third and fourth transistors comprises a source, the source of the first and third transistors being coupled together and the sources of the second and fourth transistors being coupled together, the

mixer further comprising a fifth switch coupled to the common sources of the first and third transistors, and a sixth switch coupled to the common sources of the second and fourth transistors, the fifth switch being controlled by the first one of the differential control inputs and the sixth switch being controlled by the second one of the differential control input.

75. The mixer of claim 74 further comprising a buffer to convert voltages at the first and fourth outputs to a first current and voltages at the second and third outputs to a second current.

76. A mixer, comprising:

track and hold means for tracking and holding a first signal in response to a second signal; and

limiting means for limiting the response of the track and hold means to a frequency band, the first signal being within the frequency band.

77. The mixer of claim 76 further comprising means for buffering first signal before being applied to the track and hold means.

78. The mixer of claim 76 wherein the track and hold means comprises first and second output signals, the mixer further comprising means for combining the first and second output signals.

79. The mixer of claim 76 wherein the limiting means comprises an inductor and capacitor each being coupled to the track and hold means.

80. The mixer of claim 76 wherein the track and hold means comprises a switch in a path of the first signal, the switch being controlled by the second signal.

81. The mixer of claim 80 wherein the switch comprises a transistor having a gate coupled to the second signal.

82. The mixer of claim 81 wherein the transistor further comprises a source coupled to the first signal.

83. The mixer of claim 82 wherein the transistor further comprises a drain, and the limiting means comprises a capacitor coupled to the drain.

84. The mixer of claim 83 wherein the limiting means further comprises an inductor coupled to the source of the transistor.

85. The mixer of claim 82 wherein the bandpass circuit further comprises an inductor coupled to the source of the transistor.

86. The mixer of claim 85 wherein the transistor further comprises a drain, and the bandpass circuit comprises a capacitor coupled to the drain.

87. The mixer of claim 76 wherein the track and hold means comprises a transistor having input means for receiving the first signal and output means for generating an output signal in response to the first signal, and a switch in a path of the output signal, the switch being controlled by the second signal.

88. The mixer of claim 87 wherein the switch comprises a second transistor having a gate coupled to the second signal.

89. The mixer of claim 88 wherein the second transistor further comprises a drain coupled to the output of the transistor.

90. The mixer of claim 89 wherein the limiting means comprises a capacitor coupled to the output of the transistor.

91. The mixer of claim 90 wherein the second transistor further comprises a source, and the limiting means further comprises an inductor coupled to the source of the second transistor.

92. The mixer of claim 89 wherein the second transistor further comprises a source, and the limiting means further comprises an inductor coupled to the source of the second transistor.

93. The mixer of claim 92 wherein the limiting means comprises a capacitor coupled to the output of the transistor.